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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,224	01/22/2002	Hari K. Ravichandran	P2678	6880

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EXAMINER	
MATTHEW, AARON D	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,224	RAVICHANDRAN, HARI K.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/22/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/22/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: performance monitoring chip 138. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Claims 1-8 have been cancelled, in response to preliminary amendment submitted by applicant on 01/22/2002. Claims 9-12 have been examined and are discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, (U.S. 5,564,015), and further in view of Roeber et al, (U.S. 5,682,328).

Bunnell teaches a method for monitoring an execution of a program, the method comprising the steps of:

a. Obtaining a first instruction including a first address, (see col. 6, lines 54-56; a memory access instruction inherently includes an address);
b. Searching a first memory device for an entry associated with the first address, (see again, col. 6, lines 54-56);
c. When the entry in the first memory device does not exist, generating at least one probe signal, ("cache miss signal"), indicating a miss entry in the first memory device, (see col. 6, lines 58-61); and
d. Generating a temporal identifier signal that is associated with the cache miss signals, (note col. 4, lines 44-49, wherein a clock signal is associated with the cache miss signals).

Bunnell fails to teach that the probe signal and the temporal identifier signal are then stored in memory.

Roeber et al teaches a method for monitoring and analyzing system activity by recording event data along with time information associated with said event data, (see col. 3, lines 30-33 and col. 1, lines 33-35). Roeber et al, therefore, teaches the step of storing a temporal identifier signal and a probe signal, (or event data signal), in memory.

Bunnell and Roeber et al are analogous art because they are from the same field of endeavor, viz., monitoring the performance of a system by logging event data.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the step of storing the time and cache miss signals generated in Bunnell in the method taught by Bunnel, in view of the system disclosed in Roeber et al, which teaches the motivation for the storing of such information. Roeber et al teaches that time and event data should be stored in memory so that the record of events can be later analyzed to determine what actions took place at what times within the computer program being observed, (note col. 1, lines 35-39). One of ordinary skill in the art would have been motivated to store the

time and cache miss signals generated in Bunnell, in view of Roeber et al, in order to enable future analysis of cache miss activity in the system.

2. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Levine et al, (U.S. 6,067,644).

Bunnell, in view of Roeber et al, as has already been shown, teaches the steps of:

- searching a first memory device for an entry associated with the first address, (step b),
- when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device, (step c), and
- generating a temporal identifier signal that is associated with the probe signals, (step d).

Bunnell, in view of Roeber et al, fails to teach the steps of, after step (d):

- searching a second memory device for an entry associated with the first address,
- when the entry in the second memory device does not exist, generating at least one probe signal indicating a miss entry in the second memory device, and

- generating a temporal identifier signal that is associated with the probe signals.

Levine et al teaches a method of monitoring the execution of instructions in a program, including the steps of checking a second cache in the event that an entry in the first cache does not exist, (see col. 1, lines 57-61 and col. 2 lines 1-3).

Levine et al, Bunnell and Roeber et al are analogous art because they are all from the same field of endeavor, viz., monitoring and analyzing events in a computer system.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the steps of checking a second cache, in view of Levine et al, in the event that data is not located in the first cache, in the method taught by Bunnell in view of Roeber et al. Levine et al teaches that multiple caches can be used to improve system performance. In a memory hierarchy scheme, data that is most frequently accessed is held in the smaller, and thus faster, memory of the first cache. Data that is less frequently accessed can then be held in a larger, and thus slower, memory of a second cache, and data that is infrequently accessed can be held in the largest, and thus slowest, system memory, (see col. 1, lines 64-67). Data that is more frequently accessed, therefore, is access more efficiently – improving performance. One of ordinary skill in the art would have been motivated

to include a second cache in the method disclosed in Bunnell, in view of Roeber et al, in order to improve system performance. Moreover, one of ordinary skill in the art would have considered it obvious to perform the same steps in checking the second memory device as were performed in checking the first.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Razban, (U.S. 5,289,587).

Bunnell, in view of Roeber et al, fails to teach that step (a) includes the step of incrementing a program counter with the first instruction, and fails to teach that step (c) includes the step of generating a second probe signal indicating a content of the program counter.

Razban teaches a method of monitoring system activity including the step of sending a signal indicating the content of a program counter. Razban teaches that content of the program counter is provided upon execution of each instruction, (see col. 4, lines 35-38), and that the program counter value is incremented when a new instruction is initiated, (see col. 4, lines 31-34). Razban also teaches that the program counter value is sent in the event of a cache miss, (note col. 4, lines 18-22 and 53-61).

Razban, Bunnell and Roeber et al are analogous art because they are all from the same field of endeavor, viz., methods for monitoring system progress or performance.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Razban, to increment a program counter when initiating an instruction, and include a signal containing the program counter value in the event of a cache miss, in the method disclosed in Bunnell in view of Roeber et al. Razban teaches that, when monitoring a system for bugs, one of the most important elements of information to be traced is the value of the program counter, (see col. 1, lines 30-35). This value allows the monitoring system to follow the sequence of instruction execution in the program operating the system, to better be able to identify a bug in the process with a specific instruction, (see col. 1, lines 39-42). One of ordinary skill in the art would, therefore, have been motivated to include a program counter in the method of Bunnell, in view of Roeber et al, and the steps of incrementing the program counter with the initiation of an instruction and sending the program counter value along with the cache interrupt signal, in order to enable a monitoring system to identify the cache interrupt event with the specific instruction.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Mahalingaiah et al, (U.S. 5,933,626).

Bunnell, in view of Roeber et al, fails to teach a step of, before step (b):

- searching an address storage device for an entry associated with the first address,
- when the entry in the address storage device does not exist, generating at least one probe signal indicating a miss entry in the address storage memory device, and
- generating a temporal identifier signal that is associated with the probe signal.

Mahalingaiah et al teaches a method for tracing microprocessor instructions that comprises searching a TLB for an entry associated with an address, and responding to a TLB miss event, (see col. 16, lines 29-29). The TLB is an address storage device that stores the virtual-to-physical translations of the most recently accessed data blocks.

Mahalingaiah et al, Bunnell, and Roeber et al are analogous art because they all are from the same field of endeavor, viz., methods for monitoring instructions and processes in a computer system.

At the time of applicant's invention, one of ordinary skill in the art would, as has already been shown, would have considered it obvious, in view of Bunnell and Roeber et al, to search a memory device for an entry associated with an address, and generate time and cache miss signals if the entry does not exist. One of ordinary skill would have also considered it obvious to use an address storage device, as taught in Mahalingaiah et al, in the method disclosed in Bunnell, in view of Roeber et al. The TLB disclosed in Mahalingaiah et al, provides a more efficient means of storing those addresses that were most recently accessed. If the data associated with an address is very large, efficiency can be improved in a caching system by storing only a new physical address location, in a TLB, that is associated with the most frequently or recently accessed data. Replacing address entries in the TLB would require less processing power than replacing data entries in a cache. One of ordinary skill in the art would, therefore, have been motivated to include the steps of searching an address storage device for an entry associated with a first address, before searching a first memory device, in order to improve efficiency in the system. Moreover, one of ordinary skill would have considered it obvious to check the address storage device with the same method used to check the first memory device.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 9 and 11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,341,357 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the methods disclosed in claims 9 and 11 would have been obvious to one of ordinary skill in the art in view of the functionality of the apparatus disclosed in claim 1.

Regarding claim 9, claim 1 teaches the following:

- Occurrence of a memory access miss, (line 6), which inherently comprises the steps of, obtaining a first instruction including a first address, and searching a first memory device for an entry associated with the first address;
- When an entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device, (lines 4-6);

- Generating a temporal identifier signal that is associated with the probe signals, (lines 7-9); and
- Storing the temporal identifier signal and the probe signals in memory, (lines 10-13).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the elements of the apparatus disclosed in claim 1, as mentioned above, into a method as disclosed in claim 9, as it is a direct utilization of the functionality the apparatus of claim 1.

Regarding claim 11, claim 1 teaches the following:

- Searching a second memory device for an entry associated with the first address, (lines 14-16);
- When the entry in the second memory device does not exist, generating at least one probe signal indicating a miss entry in the second memory device, (lines 17-20); and
- Generating a temporal identifier signal that is associated with the probe signal, (lines 22-23).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the elements of the apparatus disclosed in claim 1, as mentioned above, into a method as disclosed in claim 11, as it is a direct utilization of the functionality the apparatus of claim 1.

6. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 6,341,357 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the method disclosed in claim 10 would have been obvious to one of ordinary skill in the art in view of the functionality of the apparatus disclosed in claim 6.

   Regarding claim 10, claim 6 teaches the following:

   - A program counter included in a processor with a first memory device, (lines 2-4; it is well known in the art that a program counter is incremented upon initiating any new instruction);
   - Generating a second probe signal indicating a content of the program counter, (line 5).

   At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the elements of the apparatus disclosed in claim 6, as mentioned above, into a method as disclosed in claim 10, as it is a direct utilization of the functionality the apparatus of claim 6.

7. Claim 12 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,341,357 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the method disclosed in claim 12 would have been obvious to

one of ordinary skill in the art in view of the functionality of the apparatus disclosed in claim 4.

Regarding claim 12, claim 4 teaches the following:

- A TLB generating a TLB miss signal, (lines 3-4; a TLB is an address storage device, and the function of generating a TLB miss signal presupposes the steps of searching an address storage device for an entry associated with a first address);
- When the entry in the address storage device does not exist, generating at least one probe signal indicating a miss entry in the address storage memory device, (line 6);
- Generating a temporal identifier signal that is associated with the probe signal, (lines 8-9).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the elements of the apparatus disclosed in claim 4, as mentioned above, into a method as disclosed in claim 12, as it is a direct utilization of the functionality the apparatus of claim 4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (703) 605-1211. The examiner can normally be reached on Mon-Fri, from 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aaron D Matthew
Examiner
Art Unit 2114

ADM

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